CLAIM AMENDMENTS:

The following listing replaces all previous versions of the claims:

1-15. (Cancelled)

16. (Currently amended) A semiconductor device, comprising:

a solid state device having a surface and an external connection surface which is a surface on a side opposite the surface,

a semiconductor chip having a functional surface,

a connecting member provided between the surface of the solid state device and the functional surface of the semiconductor chip, the connecting member extending over a distance between the surface of the solid state device and the functional surface of the semiconductor chip and having a constant width,

an insulating film provided on the surface of the solid state device, the insulating film having an opening greater in size than the semiconductor chip, and

a sealing layer that completely seals the opening and a space between the solid state device and the semiconductor chip,

wherein a lateral distance between an outer periphery of the semiconductor chip and an edge of the opening of the insulating film is 0.1 mm or more.

17. (Previously presented) The semiconductor device according to claim 16, wherein a connection pad is provided on the surface of the solid state device.

18. (Previously presented) The semiconductor device according to claim 17, wherein the connecting member includes the connection pad.

19. (Previously presented) The semiconductor device according to claim 17, wherein the solid state device and the semiconductor chip are bonded by means of the connecting member including the connection pad with a predetermined interval between the solid state device and the semiconductor chip.

20. (Previously presented) The semiconductor device according to claim 16, wherein the solid state device and the semiconductor chip are electrically connected together.

21. (Previously presented) The semiconductor device according to claim 16, wherein the insulating film is a solder resist film.

22. (Previously presented) The semiconductor device according to claim 16, wherein the insulating film has a thickness smaller than an interval between the surface of the solid state device and the semiconductor chip.

23. (Previously presented) The semiconductor device according to claim 16, wherein the opening of the insulating film is formed so that the semiconductor chip completely falls laterally within the opening.

24. (Cancelled).

25. (Previously presented) The semiconductor device according to claim 16,

wherein the sealing layer is provided in such a manner as to fill the opening with the sealing layer, and

wherein the sealing layer serves to seal a gap between the solid state device and the semiconductor chip and to protect the functional surface, the connecting member and an exposed part of the surface of the solid state device exposed from the opening of the insulating film.

26. (Previously presented) The semiconductor device according to claim 16, wherein an end electrode that is electrically connected to the connecting member is formed at an end of the solid state device.

27. (Previously presented) The semiconductor device according to claim 26, wherein the end electrode leads from the surface to the external connection surface via an end face on the solid state device.

28. (Previously presented) The semiconductor device according to claim 26, wherein the semiconductor device can establish an electric connection with other wiring board in the end electrode.

29. (Previously presented) The semiconductor device according to claim 16, wherein the semiconductor chip includes two or more semiconductor chips each connected to the solid state device in a flip chip manner.

30. (Previously presented) The semiconductor device according to claim 29, wherein the opening of the insulating film includes two or more openings each completely laterally including each semiconductor chip.

31. (Previously presented) The semiconductor device according to claim 16, wherein the semiconductor chip has the functional surface only on one surface of the semiconductor chip.

32. (Currently amended) The semiconductor device according to claim 16, wherein [[the]] a functional ~~surface~~ element is not formed ~~not entirely~~ on [[one]] an entirety of the functional surface of the semiconductor chip.

33. (Previously presented) The semiconductor device according to claim 16, wherein the sealing layer is not on the insulating film.

34. (Previously presented) The semiconductor device according to claim 16, wherein the sealing layer at least partially covers a side surface of the semiconductor chip.

35. (Previously presented) The semiconductor device according to claim 34, wherein the sealing layer does not reach an upper surface of the semiconductor chip.

36. (Previously presented) The semiconductor device according to claim 35, wherein the sealing layer is not on the insulating film.

37. (Previously presented) The semiconductor device according to claim 16, wherein no other wiring than a connection pad for connection with the

semiconductor chip is provided on the solid state device in the opening of the insulating film.

38-102. (Cancelled).

103. (New) A semiconductor device, comprising:

a solid state device having a surface and an external connection surface which is a surface on a side opposite the surface,

a semiconductor chip having a functional surface,

a connecting member provided between the surface of the solid state device and the functional surface of the semiconductor chip, the connecting member extending over a distance between the surface of the solid state device and the functional surface of the semiconductor chip and having a constant width,

an insulating film provided on the surface of the solid state device, the insulating film having an opening greater in size than the semiconductor chip, and

a sealing layer that completely seals the opening and a space between the solid state device and the semiconductor chip,

wherein the sealing layer does not cover an upper surface of the insulating film and the sealing layer covers a side face of the semiconductor chip

up to a middle portion of the side face with respect to a thickness direction of the semiconductor chip.